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100G CFP2 ER4 Dual Rate Transceiver
Hot Pluggable, Duplex LC, EML LAN-WDM, Single Mode, 40KM, DDM

Part Number: FCF2-K7-L13-40DR

Overview

FCF2-K7-L13-40DR is a parallel fiber optical transceiver module for 100Gbit/s data transmission applications at 1300nm LAN-WDM. It is ideally suited for 100GbE Datacom, Storage Area Network (SAN) and OTN Telecom applications based on IEEE 802.3ba 100GBase Ethernet and OTN OTU4 standards. The transceiver incorporates a 4-channel laser drivercircuit together with a 4-channel EML LAN-WDM array coupled with an optical multiplexer. On the receiver side,an optical de-multiplexer is coupled with a 4-channel photodiode array and a 4-channel APD array resulting in acompact module for an aggregate bandwidth of 11.8Gb/s.

Applications

- 100GBASE-ER4 Ethernet
- OTN OTU4 Application
- Data Center
- Datacom/ Telecom Switch & Router

Features

- Compliant to CFP2 MSA
- Compliant to IEEE802.3ba 100GBase-ER4 and ITU-T G.709/Y.133 standards
- Electrical interface compliant with CFP2 MSA
- 4-CH optical Mux/DeMux design
- Support up to 112Gb/s aggregate bit rate
- Electrical serial data rate up to 27.9525Gbps
- EML LAN-WDM array transmitter
- APD receiver
- Duplex LC connector
- MDIO interface for management and diagnostic monitor
- Built in quad Tx CDR and Rx CDR
- Single 3.3V power supply
- Low power consumption, <12W
- Link length up to 40km over single mode fiber
- All metal housing for superior EMI performance
- RoHS compliant

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Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-40	+85	°C
Storage Relative Humidity	RH	5	85	%
Supply Voltage	V_{CC3}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.135	+3.3	+3.465	V
Supply Current	I_{CC}			2700	mA
Module Total Power	P			9.5	W
Aggregate Bit Rate	BR_{AVE}		103.125	111.810	Gb/s

Transmitter Electro-optical Characteristics

V_{CC}= 3.135V to 3.465V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Signaling Rate, each lane	DR		25.78125	27.9525	Gb/s	
Rate Tolerance		-100		+100	ppm	
Total Launch Power (100GbE)				+8.9	dBm	
Total Launch Power (OTU4)				+8.9	dBm	
Average Launch Power, each Lane	P_{AVG}	-2.9		+2.9	dBm	1
Optical Modulation Amplitude, each Lane (OMA)	P_{OMA}	+0.1		+4.5	dBm	
LAN WDM Each LANE Optical Wavelength Range	λ_{L0}	1294.53	1295.56	1296.59	nm	
	λ_{L1}	1299.02	1300.05	1301.09	nm	
	λ_{L2}	1303.54	1304.58	1305.63	nm	
	λ_{L3}	1308.09	1309.14	1310.19	nm	
Spectral Width (-20dB)	$\Delta\lambda$			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Extinction Ratio	ER	8			dB	
Difference in Launch Power between any Two Lanes (OMA)				3.6	dB	

Transmitter Dispersion Penalty, each Lane	TDP			3.5	dB	
Optical Eye Mask {X1,X2,X3,Y1,Y2,Y3}		{ 0.25, 0.4, 0.45, 0.25, 0.28, 0.4 }				
Average Launch Power OFF, each Lane	P_{OFF}			-30	dBm	
Relative Intensity Noise	RIN			-130	dB/Hz	
Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-12	dB	
Single Ended Data Input Swing	V_{SED-IN}	85		900	mV	
Control I/O Voltage, High	V_{IH}	2.0		Vcc	V	
Control I/O Voltage, Low	V_{IL}	GND		0.8	V	

Note1: Average launch power, each lane (min) is informative for 100GbE, not the principal indicator of signal strength.

Receiver Electro-optical Characteristics

V_{CC}= 3.135V to 3.465V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Date Rate	DR		25.78125	27.9525	Gb/s	
Rate Tolerance		-100		+100	ppm	
Receiver Overload, each Lane (OMA)	P_{IN_Max}		-	+4.5	dBm	1
Receiver Sensitivity, each Lane (100GbE)	P_{IN_sen}		-	-20.9	dBm	
Receiver Sensitivity, each Lane (OTU4)	P_{IN_sen}		-	-20.7	dBm	
Receiver Sensitivity, each Lane (OMA)	P_{IN_senoma}		-	-21.4	dBm	2
Stressed Receiver Sensitivity in OMA, Each Lane				-17.9	dBm	3,4
Optical Wavelength	λ_{L0}	1294.53	1295.56	1296.59	nm	
	λ_{L1}	1299.02	1300.05	1301.09	nm	
	λ_{L2}	1303.54	1304.58	1305.63	nm	
	λ_{L3}	1308.09	1309.14	1310.19	nm	
Difference in Receive Power between any two Lanes (OMA)				4.5	dB	
Receiver Reflectance	Rrx			-26	dB	

LOS De-Assert	LOS_D			-26	dBm	
LOS Assert	LOS_A	-40			dBm	
LOS Hysteresis	LOS_{HY}	0.5			dB	
Single Ended Data Output Swing	$V_{SED-OUT}$	200		900	mV	

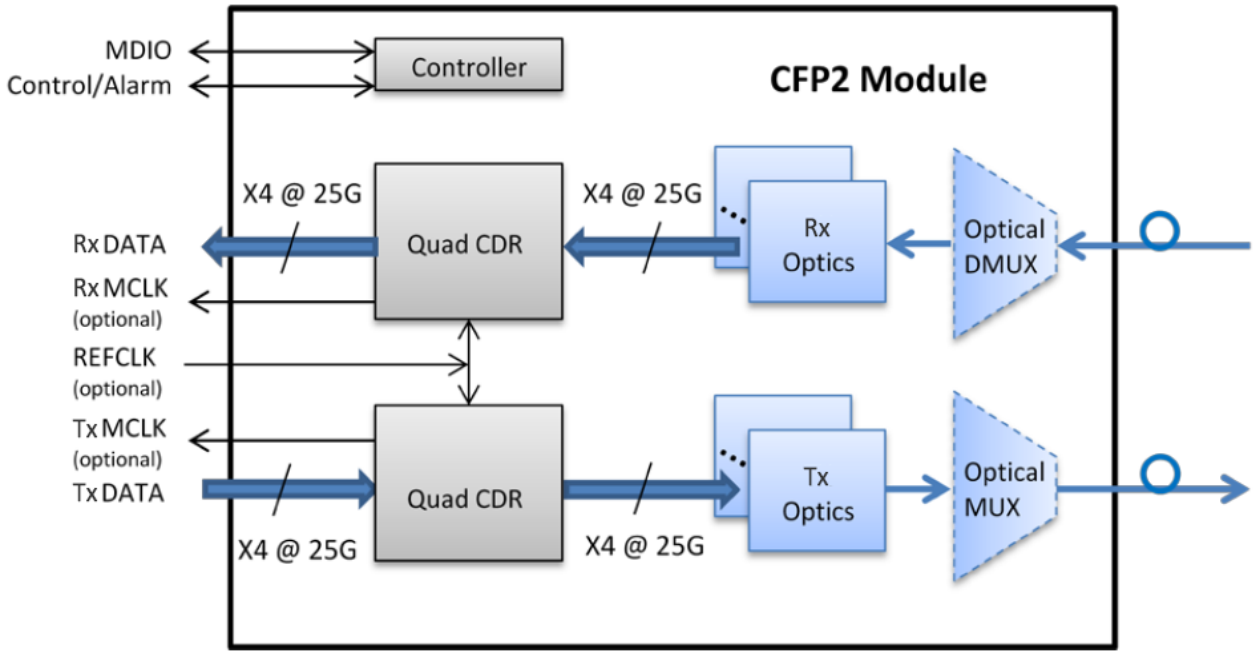
Note1: The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

Note2: Receiver sensitivity (OMA), each lane (max) is informative.

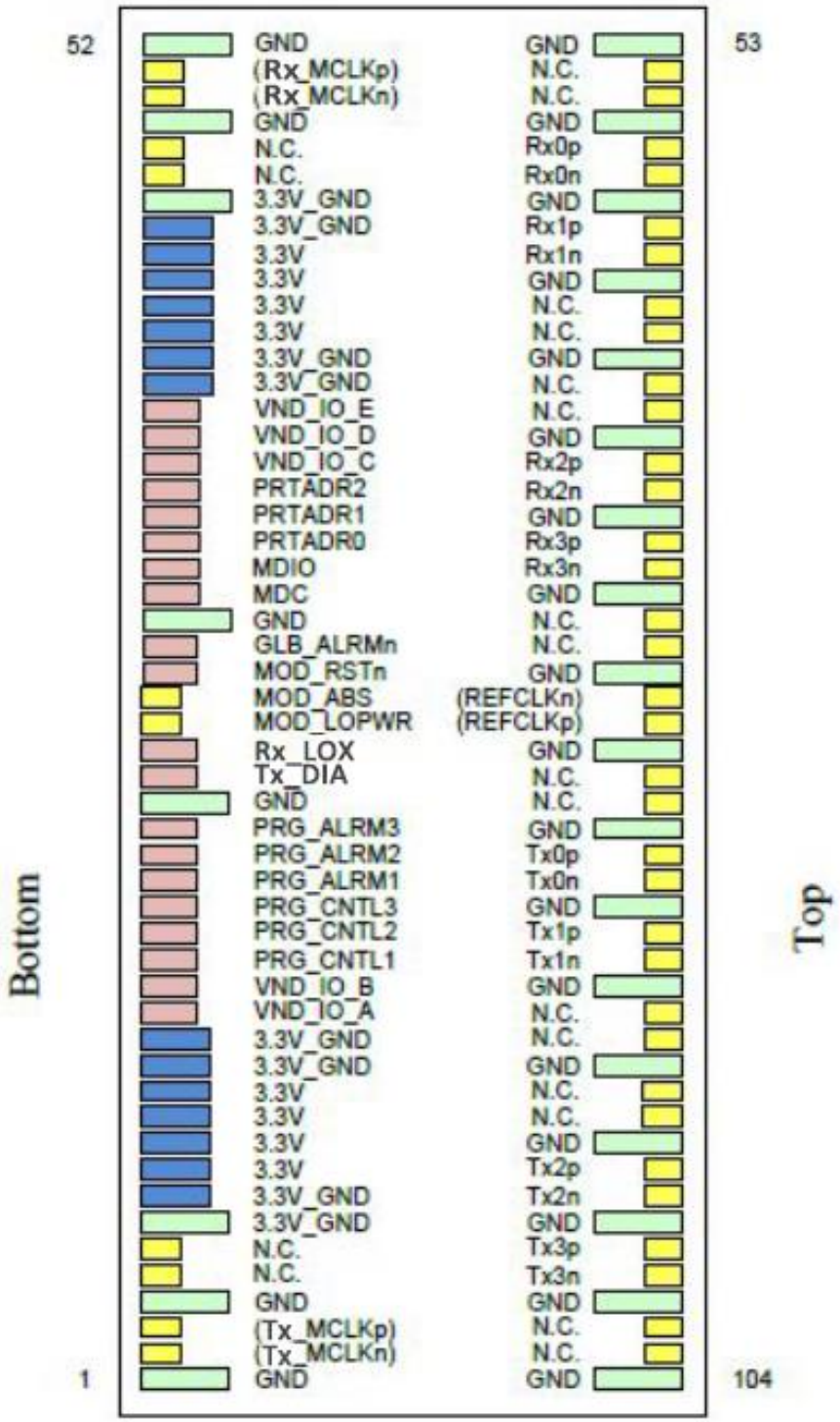
Note3: Measured with conformance test signal at TP3 for BER=10^{-12}.

Note4: conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is. 8dB;stressed eye J2 jitter for each lane is 0.3UI;stressed eye J9 jitter for each lane is 0.47UI.

Transceiver Block Diagram



Pin Assignment



Pin Description

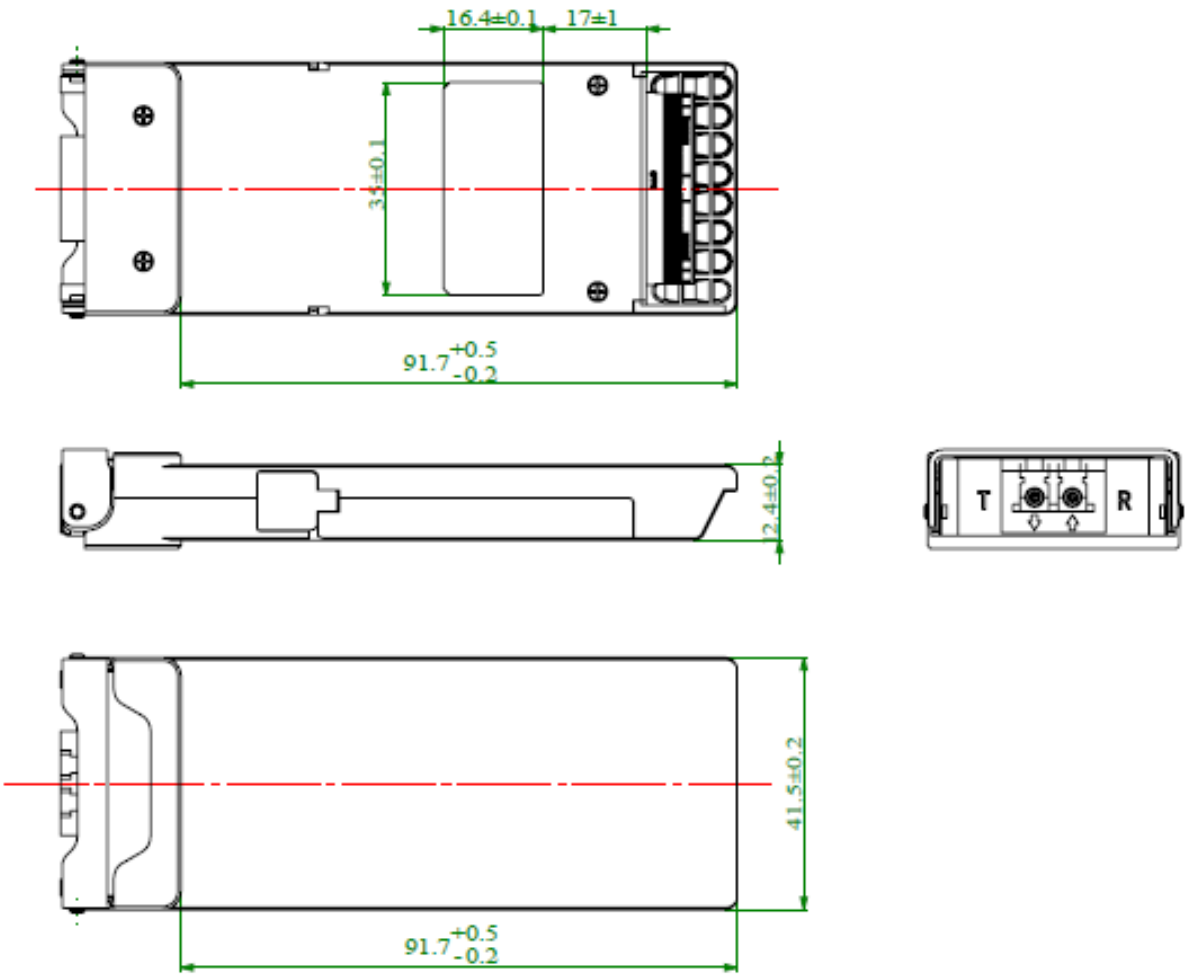
Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML	(Tx_MCLKn)	Not connect
3	CML	(Tx_MCLKp)	Not connect
4		GND	Module Ground
5		N.C.	Not connect
6		N.C.	Not connect
7		3.3V_GND	3.3V Ground
8		3.3V_GND	3.3V Ground
9		3.3V	3.3V Module Supply Voltage
10		3.3V	3.3V Module Supply Voltage
11		3.3V	3.3V Module Supply Voltage
12		3.3V	3.3V Module Supply Voltage
13		3.3V_GND	3.3V Ground
14		3.3V_GND	3.3V Ground
15		VND_IO_A	Module Vendor IO A (do not connect)
16		VND_IO_B	Module Vendor IO B (do not connect)
17	LVCMOS	PRG_CNTL1	Programmable Control 1 (MSA default: TRxIC_RSTn; “0”: reset; “1” or NC: not used)
18	LVCMOS	PRG_CNTL2	Programmable Control 2 (MSA default: Hardware interlock LSB; Default “0”: ≤ 9 W)
19	LVCMOS	PRG_CNTL3	Programmable Control 2 (MSA default: Hardware interlock MSB; Default “1”: ≤ 9 W)
20	LVCMOS	PRG_ALRM1	Programmable Alarm 1 (MSA default: HIPWR_ON; “1”: module power up completed, “0”: module not high powered up)
21	LVCMOS	PRG_ALRM2	Programmable alarm 2 (MSA default: MOD_READY, “1”: Ready, “0”: not Ready)
22	LVCMOS	PRG_ALRM3	Programmable alarm 3 (MSA default: MOD_FAULT, “1”: Fault, “0”: no Fault)
23		GND	Module Ground
24	LVCMOS	Tx_DIS	Transmitter Disable for All Lanes (“1” or NC: transmitter disabled; “0”: transmitter enabled)
25	LVCMOS	Rx_LOS	Receiver Loss of Optical Signal (“1”: low optical signal, “0”: normal condition)
26	LVCMOS	MOD_LOPWR	Module Low-Power Mode (“1” or NC: module in low power mode, “0”: power on enabled)

27	GND	MOD_ABS	Module Absent (“1” or NC: module absent; “0”: module present. Pull up resistor on host)
28	LVCMOS	MOD_RSTn	Module reset; “0”: reset the module; “1” or NC: module enabled
29	LVCMOS	GLB_ALRMn	Global Alarm (“0”: alarm in any MDIO alarm register; “1”: no alarm condition. Pull up resistor on host.)
30		GND	Module Ground
31	1.2V CMOS	MDC	Management Interface Clock Input
32	1.2V CMOS	MDIO	Management Interface Bi-Directional Data
33	1.2V CMOS	PRTADR0	MDIO Physical Port Address bit 0
34	1.2V CMOS	PRTADR1	MDIO Physical Port Address bit 1
35	1.2V CMOS	PRTADR2	MDIO Physical Port Address bit 2
36		VND_IO_C	Module Vendor IO C (do not connect)
37		VND_IO_D	Module Vendor IO D (do not connect)
38		VND_IO_E	Module Vendor IO E (do not connect)
39		3.3V_GND	3.3V Ground
40		3.3V_GND	3.3V Ground
41		3.3V	3.3V Module Supply Voltage
42		3.3V	3.3V Module Supply Voltage
43		3.3V	3.3V Module Supply Voltage
44		3.3V	3.3V Module Supply Voltage
45		3.3V_GND	3.3V Ground
46		3.3V_GND	3.3V Ground
47		N.C.	Not connect
48		N.C.	Not connect
49		GND	Module Ground
50	CML	(Rx_MCLKn)	Not connect
51	CML	(Rx_MCLKp)	Not connect
52		GND	Module Ground
53		GND	Module Ground
54		N.C.	Not connect
55		N.C.	Not connect
56		GND	Module Ground
57	CML	Rx0p	25Gbps Receiver Data Output + ; Lane 0
58	CML	Rx0n	25Gbps Receiver Data Output - ; Lane 0

Pin	Logic	Name	Function / Description
59		GND	Module Ground
60	CML	Rx1p	25Gbps Receiver Data Output + ; Lane 1
61	CML	Rx1n	25Gbps Receiver Data Output - ; Lane 1
62		GND	Module Ground
63		N.C.	Not connect
64		N.C.	Not connect
65		GND	Module Ground
66		N.C.	Not connect
67		N.C.	Not connect
68		GND	Module Ground
69	CML	Rx2p	25Gbps Receiver Data Output + ; Lane 2
70	CML	Rx2n	25Gbps Receiver Data Output - ; Lane 2
71		GND	Module Ground
72	CML	Rx3p	25Gbps Receiver Data Output + ; Lane 3
73	CML	Rx3n	25Gbps Receiver Data Output - ; Lane 3
74		GND	Module Ground
75		N.C.	Not connect
76		N.C.	Not connect
77		GND	Module Ground
78	CML	(REFCLKp)	Module Reference Clock (no connect)
79	CML	(REFCLKn)	Module Reference Clock (no connect)
80		GND	Module Ground
81		N.C.	Not connect
82		N.C.	Not connect
83		GND	Module Ground
84	CML	Tx0p	25Gbps Transmitter Data Input + ; Lane 0
85	CML	Tx0n	25Gbps Transmitter Data Input - ; Lane 0
86		GND	Module Ground
87	CML	Tx1p	25Gbps Transmitter Data Input + ; Lane 1
88	CML	Tx1n	25Gbps Transmitter Data Input - ; Lane 1
89		GND	Module Ground
Pin	Logic	Name	Function / Description
90		N.C.	Not connect

91		N.C.	Not connect
92		GND	Module Ground
93		N.C.	Not connect
94		N.C.	Not connect
95		GND	Module Ground
96	CML	Tx2p	25Gbps Transmitter Data Input + ; Lane 2
97	CML	Tx2n	25Gbps Transmitter Data Input - ; Lane 2
98		GND	Module Ground
99	CML	Tx3p	25Gbps Transmitter Data Input + ; Lane 3
100	CML	Tx3n	25Gbps Transmitter Data Input - ; Lane 3
101		GND	Module Ground
102		N.C.	Not connect
103		N.C.	Not connect
104		GND	Module Ground

Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Tx	Link	DDM	Temp.
FCF2-K7-L13-40DR	LAN-WDM 1295nm,1300nm,1304nm,1309nm	SMF 40km	Yes	0~70°C